Annual Work Programme 2010

Preface

This Annual Work Programme for 2010 elaborated by the Industry and Research Committee as per the STATUTES OF THE ENIAC JOINT UNDERTAKING Art. 9.2(b) is approved by the Public Authorities Board.

It is based on a first proposal prepared by the AENEAS association of R&D actors in the field of ENIAC Joint Undertaking, further edited under the responsibility of the Executive Director, also taking into account inputs from various Public Authorities, expressed in written (in Non-Papers), in the Board meetings and in bilateral exchanges. AENEAS has organized an Indian Summer Camp on September 9th and 10th 2009, where topics for the 2010 Annual Work Programme were discussed.

The Annual Work Programme is to be read in conjunction with the Strategic Research Agenda of the European Technology Platform ENIAC; the draft-edition of the ENIAC Multi-Annual Strategic Plan issued in November 2009, and Council Regulation 72/2008 of December 20, 2007, describing the rules and procedures of the ENIAC Joint Undertaking.

Content

1 Introduction

1.1 The context

Nanoelectronics create the essential hardware enabler for innovative electronic products and services in key growth markets for the European industry.
The European champions lost 30% of their market share in the last 5 years. In 2009, only one European player is classified among the 10 leading companies in semiconductors. The goal to sustain a leadership position for Europe requires a concentrated effort, and innovative approaches.
Following the directions defined in the Strategic Research Agenda of the European Technology Platform ENIAC, the way ahead will be based on building new public-private partnerships in the form of Joint Technology Initiatives. In its proposal to the European Council, the European Commission identified the "Keys for success" of the JTIs: in addition to clearly defined Governance and recognition of the role of the Member States in the decision-making process, they include
"*Additionality:* Each JTI must be able to demonstrate how its establishment will lead to additional research being undertaken by industry…
Market failure: Each JTI is expected to provide details of the nature and extent of market failure in the areas it is addressing and to demonstrate how public intervention through a public-private partnership will overcome the market failure effectively and will achieve the desired economic and social effects."[1]
These requirements having been fulfilled, the Council Regulation (EC) No 72/2008 set up the ENIAC Joint Undertaking for the implementation of the Joint Technology Initiative in nanoelectronics in order to create a sustainable public-private partnership and increase and leverage private and public investment in the sector.
The main objective of the ENIAC JU, as established by the Basic Act, is to contribute to the development of "key competencies for nanoelectronics across different application areas in order to strengthen European competitiveness and sustainability and allow for the emergence of new markets and societal applications".
In 2008, first year of operation of the ENIAC JU, a Call for Proposals was launched on 8 May closing on 3 September. Seven projects in the areas of research opened in the call have been selected for funding, as follows:

- E3Car, Nanoelectronics for an energy efficient electrical car
- MODERN, MOdeling and DEsign of Reliable, process variation-aware Nanoelectronic devices, circuits and systems
- IMPROVE, Implementing Manufacturing science solutions to increase equipment PrOductiVity and fab pErformance
- SmartPM, Smart Power Management in Home and Health
- SE2A, Nanoelectronics for Safe, Fuel Efficient and Environment Friendly Automotive Solutions
- LENS, Lithography Enhancement towards Nano Scale
- JEMSiP_3D, Joint Equipment and Materials for System-in-Package and 3D-Integration

In 2009, the Call has been launched on 19 March 2009 and closed on 3 September 2009. Currently, 11 proposals have been selected and the Grant agreements negotiated.

End of 2009, work was started to provide a clearer picture of the objectives and contents of the – in parallel running – initiatives ENIAC and CATRENE. Both are aiming to strengthen European competitiveness in Nanoelectronics, but show some differences in prioritization. It is expected, that the “delineation” between CATRENE and ENIAC will be realized in the Annual Work Programme 2011. Criteria for the delineation will probably be the focus on socio-economic challenges, Pan-European interest, standardization issues and strategic industrial considerations.

[1] http://cordis.europa.eu/fp7/jtis/about-jti_en.html

1.2 The JU research strategy

In the statutes of the ENIAC JU, the Multi-Annual Strategic Plan (MASP) defines the strategy that the JU will follow to ensure that the Research Agenda (RA) can be executed under the most favorable conditions. According to the statutes of ENIAC JU, article 9.2 (a), this RA is included in the MASP.

The draft MASP 2009 identifies a few, but strategically decisive, application driven key areas of research and innovation that have the potential to strengthen the European industry. To this effect, the MASP identifies the most important challenges to address from the economic, societal and political viewpoint and selects the most promising ones in terms of market success and lasting impact. The selected topics ensure a broad participation of the Member States. They encompass the complete value chain, from technology development to applications that would yield commercially successful products. In line with the objectives of a Joint Technology Initiative, offering the potential for larger Europe-wide initiatives, with more flexibility, increased efficiency, no restriction in duration or size, it is expected that large, integrated projects are launched having a significant industrial impact.

Within each integrated project, a realistic representation should be found for the underlying nanoelectronics R&D ecosystem in Europe, including large corporations, SME's, institutes, and universities. The mechanisms to accommodate smaller partners, SME's, institutes or universities in larger integrated projects shall be kept flexible e.g. by allowing direct participation in the project, special links with one of the direct project partners, or a set of linked smaller projects. These characteristics should be reflected in the 2010 Call.

2 R&D priorities for 2010

2.1 SP1 - Automotive & Transport

Introduction
In the latest version of the Multiannual Strategic Plan (MASP), two Grand Challenges have been identified, which cover the most urgent priorities in the field of Automotive and Transport. These are the "full electric car" and the "safe car". The focus of the research and development activities as defined in the MASP is expected to be in the context of the two Grand Challenges.

Target activities
As the main types of activities are derived from (long term) roadmaps[2] the key elements are mainly the same as described already in the 2009 Annual Work Program; they are:

- **Components and miniaturized (sub)systems for Assisted driving** to increase car safety and reduce collision risk.
- **Power and high voltage electronics and smart miniaturized systems for hybrid and electrical cars.**
- **Development of fail safe and fault tolerant components and electronic (sub)systems** as a cross functional priority, which applies to all existing car electronics, and to all technologies to be developed in the above mentioned topics.

Two major initiatives were launched in these fields in 2008, which finally started in 2009:

- The project **E3Car:** Nanoelectronics for an energy efficient electrical car. The objective of the E3Car project is the development of nanoelectronics technologies, devices, circuits architectures and modules for electrical cars/vehicles and demonstration of these modules in a final systems. The project considers both vertical integration with the final user and equipment providers and horizontal cooperation to build a solid nanoelectronics technology base for Europe electrical car industry and establish standard designs and platforms for electrical/hybrid cars.
- **The project SE2A:** Nanoelectronics for Safe, Fuel Efficient and Environment Friendly Automotive Solutions**.** The objective of the SE2A project is to create an integrated automotive control platform, enabled by breakthroughs in the areas of efficient fuel consumption, reduced CO2 emission and safe driving, to be achieved by the development of nanoelectronics components, subsystems and architectures. The project addresses the definition of carriers and specifications, the design and development of optimized control systems, the development of novel automotive process technologies and their integration into (sub)systems, design for reliability, test and yield, prototyping and functional verification of the project objectives.

Synergy with other priorities
Possible synergy areas with other priorities are (not exhaustive):

- Basic power and power management technology will also find use in the Sub-Programme "Energy Efficiency" for the control of Industrial Electronics.
- Safe design methodology, and Design for Reliability can profit from the results of the corresponding work in the Sub-Programme "Design Methods and Tools""
- System-in-Package technology will profit from the results of the priority "Assembling technology for system-in-package" in the Sub-Programme "Equipment and Materials", even if it will require a dedicated effort for temperature control and heat management

[2] Technology Platform for Automotive ERTRAC; SRA of the eRTD WG of the eSafety Forum

Expected impact

Expected industrial impact relates directly to increased competitiveness of the semiconductor and the automotive industry in key lead markets. Other closely related industries such as avionics, industrial electronics or industrial equipment operating in harsh environments or requiring high reliability considerations will also benefit.
Direct social impact is also expected on mobility policy, safety and on sustainability (environmental) policies.

Targeted Approach

Large scale projects were targeted in 2008 developing basic technology up to a final system demonstration, involving the cooperation of user companies (automotive equipment and car manufacturers), semiconductor companies, design houses, assembling and packaging companies and relevant research institutes and universities. These projects should show both vertical integration with the final user and with equipment, materials and design providers and horizontal cooperation to build a solid technology base for Europe and establish standards.

Projects proposed for 2010 will focus on R&D activities, which will continue those started in E3Car and SE2A. In addition to this, there will be complementary activities like car lighting. This will give additional opportunities especially for SME's and research institutes to contribute by filling technology or capability gaps, or to explore initial research by feasibility studies or in different applications.

Possible topics of projects

- Serving the Grand Challenge "Full Electric Car"
  - Architectures of the fully integrated energy supply for single or distributed propulsion systems.
    Exploration of the architecture and modularity of the control system as well as increase of the possible integration levels of the functionalities within the energy supply.
  - (Electronics for) smart electrical drive concepts for the full electrical powertrain
    Research on new electrical machine concepts with novel architectures and materials, the power electronics packaging and cooling for in-motor integration up to the subsystems, systems and vehicle demonstrators, addressing the full supply chain of electric drives for automotive.
  - Solid state lighting systems for automotive applications
    Definition of relevant solutions at system level by addressing the whole automotive lighting value-chain - ranging from IC manufacturers to car makers.
  - Smart sensor nodes for automotive
    Sensors will be simulated, developed and tested with respect to safety, EMC, reliability and all other aspects to survive for at least 11 years in the car. As a result, sensors for automotive are (multi) sensor solutions with pre-processing encapsulated into dedicated modules.

- Serving the Grand Challenge "Safe Car"
  - Smart sensor nodes for automotive (belongs also to "Full Electric Car")
    Sensors will be simulated, developed and tested with respect to safety, EMC, reliability and all other aspects to survive for at least 11 years in the car. As a result, sensors for automotive are (multi) sensor solutions with pre-processing encapsulated into dedicated modules.
  - Advanced radar and time-of-flight
    Development of novel radar and time-of-flight sensors, which shall be affordable, generic, multipurpose, and integrated to the vehicle systems, and not restricted by future frequency allocations.

2.2 SP2 - Wireless Communications

Introduction
We are now in a highly moving world where mobility, connectivity and data processing are ubiquitous. The strong position of Europe today in wireless communications needs to be reinforcing in the future to guarantee its competitiveness and make sure the industry based on nanotechnology, and all the value chain relying on it, will remain a substantial source of value and employment.

Target activities
The convergence scenario of consumer, computer and communication electronic systems requires an exponential growth of code and data in all electronic systems. In this context, the digital CMOS, (logic & memories) technology will be still dominant but the traditional Moore's law based integration increased will be only a part of the solution to a complex problem. Because of power consumption, flexibility, size and cost, the next generations of wireless systems will require new technologies and architectures that combine adaptability and performances in a novel way. To tackle these new challenges, a specific attention has to be paid on CMOS ultra low power, CMOS compatible 3D processes, thin film technologies, (SOI, Thin FET…) RF and Analog mixed signal and memories technologies as well as silicon photonics. In other hand due to more communications applications, more mobile users and more distributed data, a new security paradigm is requested.
To address these new technologies, three Grand Challenges have been identified requesting a long range planning effort and close cooperation along the whole value chain. The three Grand Challenges are namely**:**
I) ***Front End & Back End heterogeneous 3D integration Platform***
Objective: To enable the development of Materials, design tools and design methodology, manufacturing equipments and manufacturing process for Heterogeneous integrations.
II) ***Technologies for "Green" Wireless Communication*****:**
Objective: From the system level to the design implementation to deploy in a holistic approach green wireless solutions.
III) ***Agile radio & security issues***
Objective: To develop innovative integrated design solutions for both the RF front-end and the digital baseband

Synergies with other priorities
Synergies with Sub-programmes 4,5 & 6 are:
- Energy efficient design
- Design efficiency for heterogeneous design (e.g. Design kit for 3D integration)
- Technologies for heterogeneous integration
- Equipment, Materials and Manufacturing for More than Moore innovation
- Equipment, Materials and Manufacturing for 3D Manufacturing

Expected impact
To spur the development of innovative and cost effective technologies, enabling designing and manufacturing in high volume silicon systems solutions for the wireless communication market.

Targeted Approach
It is expected that the projects addressing the wireless communications domains will be formed with consortia combining the expertise of large firms, SMEs and Academic research centers.

Possible topics of projects

Design kit for 3D integration

- 3D floor-planner with multi-CMOS technologies in one framework, able to interface with 2D tool for IC physical implementation, DFM rules, 3D library, system partitioning, Electrical characteristic, ESD strategies

3D Heterogeneous integration

- Integrated passive-RF-sensors-opto- including packaging issues and accurate models
- Memory systems
- Quality enhancement and Failure Analysis- Fault isolation methods
- Design for Failure Analysis: Design verification & debug.

Agile Radio

- Smart SDR system/Sensing: - spectrum issues- sensing algorithm.
- Dynamic reconfigurable architecture

Agile RF transceiver

- Reconfigurable antennas with MEMS switches. – Multipath Mimo solutions
- Highest integration of PA and Digital enhanced RF

Green wireless

- Holistic approach Energy management at different level (Chip / terminal / network) – Measurements, estimation
- Power driven design: H/S power profiling issues - Ultra low power technologies
- Energy harvesting techniques

Security

- Open trusted platform
- Identification and authentication
- Secure storage
- Adaptable security features
- Formal tools for security and embedded software test verification

New Memory System for Wireless Communications

The research activities will cover new Hardware and Firmware technologies including packaging issues for mobile systems and communication of large and multi-form data assistant (mobile phones, PDA, laptops etc.) allowing them also to bridge to the wired network in the house.

2.3 SP3 - Energy Efficiency

Introduction

Efficient generation, distribution and use of energy are key for the solution of the two Grand Challenges as they have been described in the MASP. These Grand Challenges are "CO_2-Reduction" and the "Smart Energy Grid". Focusing on micro-/ nanoelectronics approaches, efficient power supply and intelligent energy control in new products can reduce electrical energy consumption in Europe by 20% to 30 % until 2020 by simultaneous increase of safety, functionality and convenience. This will reduce CO_2 emission in the same order of magnitude in order to achieve the Kyoto protocol targets and will limit the energy cost increase.

Target activities

Provide innovative technologies as the basis for new energy efficient products and intelligent power management to enable increased competence in these emerging lead markets in line with the 'sustainability' objective[3].

Industrially driven projects for Nanoelectronics Research for Energy and Environment addressing the areas of **intelligent drive control** including technology, components and miniaturized (sub)systems addressing the challenges at system and device level for highly efficient controlled engines and electrical actuation in industrial applications and efficient **power supplies** and **power management solutions,** combining the measures for voltage conversion and stand-by were called for in 2008.

One large initiative was launched in 2008. The project **SmartPM** dealing with Smart Power Management in Home and Health**.** The objective of the SmartPM project is to develop application-specific, efficiency-optimized semiconductor power technologies enabling actual deployment of intelligent systems in large-scale, energy-critical application fields like home and health. Applications in these fields require innovative system architectures and circuit designs, new components, efficient power electronic technologies, and innovative module, interconnect and assembly technologies. An important aspect is the support and the compatibility of upcoming legislation and regulations for efficient use of energy. The SmartPM will develop the semiconductor technologies and module platforms enabling intelligent motor drives for highly controlled engines and efficient power supplies and power management solutions.

In 2010, additional activities are looked for to complement and/or enhance the potential and impact of the activities launched in 2008. Such additional activities must target **low power consumption of the circuits** and their **interaction in different applications.** They can address **support activities** such as characterization, simulation and test.

Synergy with other priorities

Synergy could be established with other Subprograms, for the development of a common, cross-functional technology base. Possible synergy areas with other priorities are:

- Power management technology and intelligent drive control will also be used in the Sub-Programme "Automotive and Transport".
- Synergies with design platform activities in the design of efficient power supplies, high reliability solutions, design for operation under harsh conditions.
- Synergies with equipment and materials in relation to high power electronics. Completely new or improved semiconductor technologies, using leading edge technology knowledge for low power consumption and extended lifetime (e.g. high frequent and low-loss switching, digital power conversion). New semiconductor materials like SiC or GaN, thin substrates and interconnect materials to improve performance and reduce cost. In-package integration of power devices and control logic.

[3] Current Sustainable Development Strategy (2006): European Council *DOC 10917/06*

Expected impact
Direct impact is expected on the automotive industry, on automation and on industrial equipment and home appliances. Direct contribution should go to various environmental and sustainability policies at national and European level.

Targeted approach
Large scale projects were targeted in 2008 developing basic technology until demonstration in a real environment, involving the cooperation of user companies. These main projects should show both vertical integration with the final user and with equipment, materials and design providers and horizontal cooperation to build a solid technology base for Europe and establish standards.

In addition to these larger size projects led by industry core companies, additional smaller work areas are targeted in 2009. This will give additional opportunities especially for SME's and institutes to contribute by filling technology or capability gaps or to explore initial research results in different applications that appear as larger programmes develop. Smaller projects and cooperation / coordination with larger initiatives in this field is encouraged.

Possible topics of projects

- Serving the Grand Challenge "CO_2-Reduction"
  - Solar (or other alternative) energy supply chain
  - Design and demonstration of a new bunch of innovative electronic components and solar cells for higher performance photovoltaic systems.
  - System Level Power Analysis
    Development of design tools that will produce power efficient designs and applications for the emergent mobile and ubiquitous SoC computing platforms that are characteristic of many applications in the health, automobile and wireless domains.
  - Eco–logic integrated circuits
    Development of Ultra-Low Power solutions for future generation ICs by investigation of design methodologies to achieve the lowest possible power consumption and low-voltage microarchitecture
  - Novel power conversion platforms
    Power converter platforms with significantly increased conversion efficiency for convertors with a maximum power between 20 W and 2 KW and voltages between 1600 V and 12 V.
  - Piezo MEMS sensors and actuators
    Development of new sensors and actuators based on piezoelectric MEMs. This will require R&D in materials, processing, electrical & acoustical characterisation and production-readiness, as well as system design and integration.
  - Smart, networked and controlled home appliances
    Reduction of energy in the range of 30% without loosing comfort or restrictions in life quality by researching solutions for "smart, networked and controlled home appliances" for energy saving.
  - Intelligent Solid State Lighting Modules and Systems
    Development of green and intelligent SSL modules and lighting systems with integrated control sensors, lamp interfaces, SSL dimmers for general illumination purposes, which are affordable and easy to install, maintain and extend.

- Serving the Grand Challenge "Smart Energy Grid"
  Development of a new local smart grid architecture.
  Power management algorithms to reduce the total energy consumption by more than 20% over the life time. To be used by smart meters and energy management devices, systems renewable local (distributed) power generation and energy (Micro/macro), storage systems (including electric vehicles with energy generation and storage for grid operations).

2.4 SP4 - Design Methods and Tools

Introduction

This Sub-Programme is one of the three cross-functional Sub-Programmes, together with "Silicon Process and Integration" and "Equipment, Materials and Manufacturing" that aim to build the basic technology base for all application-specific technology development. Design is the key link between technology and the world of applications, but design capabilities and design cost are also seen as limiting factors for the future technological development. An enormous increase of design productivity is necessary to exploit the whole potential provided by the new attractive technologies. In addition, due to the growing difficulty to maintain the pace of progress in performance and area for future technology nodes the profitability of new products is more and more depending on the progress of design and EDA tools.

Being a crosscut technology, the impact of Design Tools and Methodology is felt mainly through its effects on innovation and productivity. The efficient use of TCAD platforms (for equipment, process, device and circuit simulation) is expected to provide a 40% cost reduction in technology development for 2007[4]

Target activities

European high tech industry has a strong position in the fields of Automotive and Aerospace, Mobile Communications, Security and Industrial, while promising areas, strongly dependent however from Public Procurement for the creation of markets, are in the field of Health, Ambient Assisted Living and Energy Efficiency. All these segments have strongly specific requirement that require the integration of logic with other functions, like RF or optoelectronic links, power devices, sensors and analogue interfaces. Most of them have also severe reliability and power efficiency requirements. On these bases, 3 "grand challenges" have been identified for research on Design Methods and Tools. Different competences need to be activated at European level, both in the industrial and in the academic world.

- **Design efficiency for functional complexity**

The main target is to organize tools and methodology in order to improve the efficiency of design of the complex devices needed for critical applications, often requiring the integration of heterogeneous logic components (microprocessor cores, DSP, memories, dedicated logic) and heterogeneous functions (RF, analogue, power) on chip or in package.

- **Reliability and yield by design**

Applications in the field of Automotive and Aerospace, Security and Health require very high levels of reliability, often for limited production volumes. Therefore testability, reliability and yield must be inserted by design. At the same time, integration of different functions and increasing weight of parasitic effects and new emerging types of production defects are introducing new causes of malfunctioning that require dedicated new DFT (Design-for-Test) measures for effective detection and screening.

- **Energy efficient design**

Energy efficiency is one of the most critical aspects of today's information society. Electronic technologies can play a fundamental role in contributing to energy savings in different domains. However semiconductor devices themselves are a source of power consumption that can be dramatically felt in battery powered devices for communications and health, but is impacting also critical components of the information society, like servers and data-centers. Therefore, adequate design automation support, offering robust and accurate modeling capabilities and computer-aided design exploration/optimization solutions is needed to reduce power consumption in electronic systems.

[4] ITRS Winter Conference, Makuhari, Japan, Dec. 2007

One major initiative was launched in these fields in the frame of the first ENIAC call:

- **MODERN**: Device, circuit, and system variability and reliability. The objective of the project is to develop new paradigms in integrated circuit design which will enable the manufacturing of reliable, low cost, low EMI, high-yield complex products using unreliable and variable devices. The main goals are modeling of process variations for nanometer devices, methods for evaluating the impact on manufacturability, reliability and performances, methods and tools to mitigate the effects of process variations and final validation on demonstrators.

Synergy with other priorities

Being an enabling Sub-Programme, "Design Methods and Tools" interacts with all other Sub-Programmes. Especially important synergies are:

- Safe design methodology, and Design for Reliability can find synergy with application projects in "Automotive and Transport".
- Low power devices, very often being used in safety or health relevant applications, will enable application in "Energy Efficiency" and "Wireless Communications"
- Failure analysis and reliability procedures related to high temperature, high current/voltage operation will also be an issue for Sub-Programme: "Automotive and Transport" and "Energy Efficiency"

Expected impact

The largest economical impact of design efficiency is on chip area, cost of design and especially time-to-market. Price drop for semiconductor devices is in the order of 27%/year. A delay of a few months in designing a new product can have a significant impact in profit margins.

There is no clear data about the weight of design resources spent in Europe. Some information can be deduced from the existing data on the market of EDA tools. Total sales (licenses plus assistance) for EDA tools in Europe was around 1 B$ in 2007. Assuming an average investment of 20-25K$ per designer, it gives a total of 40-50 thousand IC designers in Europe, distributed between semiconductor companies, fabless design houses and IP providers, and system companies. With a ratio 1:3 between EDA tool investment and other costs (salary plus design hardware), we can assume that total investment in design by European companies has been around 3.5-4 B$, or 2.5- 2.8 B€ in 2007, which represents an investment of more than 10% of the sales of European semiconductor industry.

Targeted approach

It is expected that the topics of the Sub-Programme would be covered by large scale projects, with a broad industrial participation, A critical mass is required to provide solutions that could be widely deployed in the European scenario, and to achieve a large degree of standardization in order to provide user friendly tools and methodologies that can be used also by smaller design companies and reduce costs. The cooperation of user companies (IDMs, fabless), design centers and CAD tool developers, universities and institutes in the projects will contribute to build a solid electronics design base for Europe and establish standards.
More focused and speculative projects, aiming at the exploration of new approaches, with larger academic participation will be better addressed by regular FP7 calls.
The projects could offer space to the growth of specialized EDA start-ups, also through the aggregation of smaller focused projects on the main ones.
Synergy should be established with other Sub-Programmes, since the design is an integral part of all electronics products.

Possible topics of projects

- **Methods and tools for the efficient design of complex systems**, covering exploration and optimization of different architectures, including heterogeneous components and non purely logical functions, dedicated design environments for specific applications and high level performance appraisal.
- **Reliability by design,** covering both high level design methods, including fault tolerant design methodologies, redundancy and re-configurability, and physical level optimization of design to make it robust against known failure mechanisms. Design verification and testing solutions are a natural complement to this topic.
- **Energy efficient design**, covering solutions to increase power efficiency of the electronic devices, especially through system level analysis and optimization.

2.5 SP5 - Silicon Process and Integration

Introduction

A significant part of the success of the semiconductor industry in the past decades is due to the fact that generic silicon technologies are used throughout a wide range of applications and that the associated R&D cost can be shared among many different markets. It does translate into the fact that in most cases the silicon process development in Nanoelectronics is driven by pure technological progress and can't be linked to a specific application domain. There is thus a need to identify the R&D on generic silicon process and process integration as a cross-cutting priority: This programme will allow Europe significant control over generic Si processes which will ensure progress in terms of cost, scaling, power / energy consumption and functionality and will also serve as key enablers for major European lead markets and societal challenges. Without this control, many societal issues cannot and will not be addressed.

Target activities

Industrially driven projects for Silicon Processes and Integration will address three complementary areas of More Moore, More than Moore and Heterogeneous Integration. It is only by combining and mastering these three domains that the European Nanoelectronics industry can offer competitive systems solutions to address the European needs.

- **More Moore** (MM) focuses scaling processes for digital data processing and storage. The vision in this domain is to maintain through R&D leadership the ability of the European industry to drive the development and manufacturing of advanced CMOS. Expertise and technology appropriation need to be developed in advanced CMOS and in disruptive memory technologies for stand-alone or embedded applications.
- **More-than-Moore** (MtM) addresses interfacing with the outside world and managing the energy / power consumption of the electronic system. The vision in this domain is to make Europe lead the worldwide R&D in "More-than-Moore" technologies. "More-than-Moore" is a domain initially proposed and conceptualized by Europe to stress the value and critical importance of non-digital functions in system solutions and Europe has key competitive advantages to address this field.

Heterogeneous Integration (HI) brings chips together in a single package. The vision in this domain is to develop a European System-in-Package supply chain for innovative systems integrating advanced CMOS and European "More-than-Moore". As this supply chain is not firmly established yet worldwide there is an opportunity for Europe to rebuild a "Back-End" industry. Classical assembly and packaging has moved mostly to the Far-East. By establishing its leadership in the heterogeneous integration of complex systems, Europe can regain a significant role in the worldwide "back-end" market.

Synergy with other priorities

Addressing enabling technologies, "Silicon Processes and Integration" interact with all other Sub-Programmes. Especially important synergies are on:

- low power and energy efficient technologies
- memory technologies
- RF technologies
- sensors and actuators
- 3-D integration

Expected impact

Innovations in electronics-enhanced systems and applications are enabled by mastering advanced CMOS and memory technologies. A strong European R&D programme on “More Moore” is a prerequisite to specify and access the latest technologies and thus secure further growth in European lead markets. Furthermore, progress in MtM is mostly fuelled by the development of advanced “More Moore” processes and integrating MtM devices in advanced CMOS needs an in-depth knowledge of the development of the MM devices as the MtM “add-on” will strongly affect the performance of the core CMOS devices;

By setting the pace of the “More-than-Moore” R&D worldwide, Europe can expect the same benefit as the US (and recently Asia) did in aligning the world R&D efforts in the “More Moore” domain.

3D/SiP heterogeneous integration is expected to act as a key differentiating factor of complex integrated systems. In mastering its supply chain, Europe will be able to secure its future in many application domains.

Targeted approach

It is expected that the projects addressing the silicon processes will be formed with consortia combining the expertise of large firms, SMEs and Academic research centers.

Possible topics of projects

- **CMOS R&D beyond 28nm node** including process steps and modules (e.g. advanced substrates, high k / metal gate, mobility boosters, metallization, etch, deposition and patterning) and associated modeling and characterization techniques, logic devices and associated embedded memory options, evaluation of SOI architectures and testchip design for 22nm/18nm and below. Dedicated low power / low energy technologies will be also evaluated.
- **RF silicon technologies up to the THz range** and associated design platform and characterization techniques. It may make use of advanced CMOS (e.g. sub-45nm SOI) or BiCMOS (e.g. 65nm) technologies. Advanced passives (antennas, filters, etc.) will be developed concurrently.
- **Generic processes needed for sensors and actuators**.
- **Heterogeneous integration technologies**, aiming at few driving applications (e.g. wireless, autonomous sensor network and/or energy efficiency). It will cover 3D mounting solutions (interposers, new substrates), 3D standardized back-end rules allowing a better interface between “front-end” and “back-end” lines and processes and heterogeneous integration of logic, memories, passives, rf, energy scavenging and/or generation and optical technologies with the associated modeling and characterization.

2.6 SP6 - Equipment, Materials, and Manufacturing

Introduction

The European Equipment, Materials, and Manufacturing (E&M) industry aims to provide innovative and superior elements for semiconductor manufacturing. To fulfil this mission also in the future, Grand Challenges in two fields need to be mastered. In Field 1 *"Direct Impact"*, the E&M products define a big, self-sustaining global market by themselves. In these global markets, the European E&M industry has achieved a world leading position, and acts as a powerful European engine for economic growth by itself which is underlined by the more than 100.000 individuals working in the European E&M industry today. In Field *2 "Strategic"*, small and emerging E&M markets are addressed that exhibit a high leverage to European key industries, e.g. tailored E&M solutions that enable heterogeneous integration for automotive applications. The European-wide spread of ENIAC partners will provide a very good and broad base for important European standardisation objectives connected to the introduction and market penetration of new equipment and materials for semiconductor manufacturing.

Target activities

Industrially driven projects for equipment, materials will address the following four grand challenges. In the field of "Direct impact" where the E&M products define a big, self-sustaining global market by themselves the following two grand challenges are addressed:

- **EUV and complementary 1Xnm patterning**

The vision is to realize EUV Lithography as the chip mass manufacturing technology of the next decade beginning at 22nm feature sizes (half-pitch) and complementary 1Xnm patterning technologies. Major technology solutions need to be developed: EUV infrastructure and metrology including mask fabrication processes, cleaning, inspection and review tools, sensitive resists, defect engineering and process control. Furthermore, the development of complementary 1Xnm patterning technologies as e.g. e-beam lithography is required for mask making, fast prototyping, and low-volume manufacturing.

- **450mm supply chain**

The vision is to enter 450mm arena at an early stage to create new opportunities to increase the European world wide market share in this competitive domain. The key technology target for the European companies and institutes is to develop and set common standards and strategies for 450mm Equipment, Materials, and Manufacturing. Important examples are 450mm substrates and SOI development, and the generation of an open platform for 450mm equipment.

In addition, two grand challenges are targeted in the field "Strategic" to address emerging applications that exhibit a big lever to European key industries.

- **"More Moore" innovations**

The vision is to keep the leading position of European E&M companies across the entire value chain. Accordingly, open issues in the fields of metrology, substrate, SOI, cleaning, deposition, structuring, and manufacturing efficiency are addressed in close collaboration of European E&M companies, institutes, and chip manufacturers. In particular, projects similar to the ones in the Semiconductor Equipment Assessment (SEA) scheme would give a major boost to this programme.

- **"More than Moore" innovations**

The vision is to open new market opportunities for the European E&M industry for diversified technologies (e.g. power, sensors). Therefore, the topics of metrology, substrate, SOI, cleaning, deposition, structuring, and manufacturing efficiency are targeted where close collaboration of European E&M companies, institutes, and chip manufacturers in mandatory. A particular focus will be put on solutions for small volume manufacturing, and highly diversified processes and products.

Three major initiatives were launched in these fields in the frame of the first ENIAC call:

- **IMPROVE**, Implementing manufacturing science solutions to increase equipment productivity and fab performance. The project aims to improve European Semiconductor fabs efficiency by providing methods and tools to better control the process variability, reduce the cycle time and enhance the effectiveness of the production equipment. It will focus on development of Virtual Metrology techniques, of Predictive Equipment Behaviour techniques and of concepts for Dynamic Risk Assessment and Dynamic Control Plan.
- **LENS**, Lithography Enhancement towards the nanoscale. The project aims to developing and integrating the overall infrastructure required to reach patterning resolutions required by 32nm and 22nm technology nodes through the double patterning and pitch doubling technology on existing conventional immersion exposure tools, with the purpose to allow the timely development of 32 and 22nm technology nodes for memories and logic devices
- **JEMSiP_3D**, Joint Equipment and Materials for System-in-Package and 3D-Integration - shall provide 3D integration onto non-Si and Si substrates: test equipment, measurement protocols and reliability methodologies, performance evaluation and equipment validation for volume manufacturing to implement production worthy tools for 3D integration.

Synergy with other priorities

Synergies are expected with “Design methods and tools for nanoelectronics” and “Silicon Process and integration”. Furthermore, the E&M chapter provides basic technology development for all application Sub-Programmes. Specific technologies and device options will serve certain application areas as e.g.

- Embedded non-volatile memories for automotive and security applications (SP2 and SP3)
- Low power CMOS for wireless communication, medical monitoring and ambient intelligence (SP1, SP5 and SP6)
- Silicon Carbide substrates and devices for power applications (SP2, SP4 and SP6)
- Sensor and 3-D integration for medical and ambient intelligence (SP1 and SP6)

Expected Impact

Innovation in materials, equipment and advanced process and manufacturing activities are key elements for any progress in the semiconductor Industry. Projects will need to contribute to maintain the key position of European equipment suppliers in the global market and to the competitiveness and sustainability of the semiconductor fabrication in Europe.

The grand challenges defined above address large markets, and emerging markets of strategic importance offering tailored solutions for the European chip manufacturers, respectively. The world wide E&M market has a total annual volume of ~35 Billion €. 450mm E&M may become a dominant segment in this market and forefront R&D for 450mm will create new opportunities to increase the European market share in this competitive domain. Furthermore, EUV lithography alone addresses a large market with an estimated annual volume of ~3 Billion € in 2015 with additional substantial markets for the EUV infrastructure and complementary 1Xnm patterning technologies. Finally, the strategic fields of More Moore innovations and More than Moore innovations have significant economical impact via tailored solutions for European chip manufacturers with high lever for European key industries as e.g. automotive and telecommunication.

Targeted approach

The future challenges in the “Direct impact” filed of the E&M industry are so large by themselves that they require a multi-national and multi-lateral approach to be successfully mastered. Accordingly, topics in this field are expected to be covered by large scale projects with strong industrial participation in order to allow a sufficiently wide deployment of the provided solutions.

In the “Strategic” field, a close interaction of the E&M industry with European chip manufacturers and institutes is required to develop E&M solutions that optimally serve the semiconductor industry to realize tailored solutions for other European key industries.

Possible topics of projects

EUV lithography / complementary patterning

- Tool technology and critical overall infrastructure for high volume sub 22nm EUV lithography
- scanner and source optics
- EUV mask infrastructure focusing on mask processing and mask characterization

450mm

- SoI substrates, and substrates and related technologies (bonding, cleaning, thermal treatment)
- Wafer handling platform including process and metrology prototypes

More Moore innovations

- Metrology innovation minimizing statistical errors
- In-line metrology (equally relevant for MtM innovations)
- Ecologically optimized semiconductor manufacturing (equally relevant for MtM innovations)
- Photomask innovations for better pattern fidelity (OPC, DP, SMO,..) including contamination, defect, degradation control
- 22nm optical lithography: design & data preparation, photomasks, metrology, and wafer processing; transition to EUV/e-beam (mix and match)

More than Moore innovations

- 3D IC manufacturing (through silicon vias, wafer level packaging,…)
- Efficient manufacturing of small heterogeneous lots
- Disruptive technologies for back end of line and wafer level packaging
- Industrial structuring of large area organic substrates

2.7 SP7 - Healthcare and the Aging Society

Introduction

A globally aging population, with an increasing number of patients that suffer from chronic and infectious diseases, exploding healthcare costs, growing shortage of healthcare professionals, and an empowered patient call for a number of radical changes in the way healthcare is currently delivered. This societal challenge creates opportunities for the nanoelectronics industry, as equipments and services for early diagnostics and for prevention will rely increasingly on specific electronics and sensors achieving a better efficiency at a lower cost.
Beside traditional devices and services for medical care, home care and home patient monitoring are now an essential part of modern, integrated and patient-centred health care. While the home environment is a relatively new application, also the clinical environment needs clear advancement in productivity as well as quality improvement at large. This trend will drive the development of new devices and services creating opportunities for dedicated electronics, microfluidics and micro-actuators.

Target activities

Industry driven projects for “Healthcare and the Aging Society” will address the following areas of nanoelectronics for healthcare (which can be considered as the Grand Challenges of this sub-programme):

- **Early diagnostic and prevention** will be made possible through improved biosensors and imaging systems allowing many diseases to be diagnosed – even before sufferers complain of symptoms – by 'in vitro' analysis or ‘in-vivo’ monitoring of biological samples (blood, saliva, sweat, etc.) and parameters (e.g. for cardiovascular & respiratory pathologies). Smarter, more accurate and cheaper solutions will help to spread these techniques to the physician and to the citizen (‘the doctor in your pocket’) improving compliance. Seamless communication systems will serve as a hub in the telemedicine between sensors and healthcare service providers. Highly reliable tests will identify those pre-disposed to certain diseases, allowing them to enter preventive programs that will identify early onset of the disease. Improved image detectors lead to efficient, more precise and earlier detection of diseases. These improvements incorporate increasing the resolution, supporting larger data rates, and being more precise in the properties of the signals that are detected. In addition, the detection of other kinds of signals can lead to earlier detection of symptoms, and/or reduce the harm to the patient. In this context, more precise and earlier detection also allow for significant dose reduction for a patient. For screening purposes, imaging systems without radiation have to become cheaper, faster and more accurate.
- More **targeted therapy** will be achieved by combining imaging with therapy. Image guided intervention will help in medical diagnosis, planning and treatment of patients by minimally invasive placement of diagnostic and therapeutic devices such as catheters, stents, but also heart valves inside the human body, enabled by medical image analysis and navigation methods. Testing in real time individual response to drugs will help to tune the therapeutic protocol and reduce side effects in conjunction with telemedicine for a better patient coaching. Smart devices will also help to monitor the healing process (e.g. e-Inhalers for rapid and accurate dosage of drugs, also using smart band-aid with impedance changes for wound healing). In the same way smart automated drug-delivery systems, based on MEMS actuators coupled with low power control logic and energy scavenging, will help to apply therapy where and when it is needed. Specific techniques like deep brain stimulation and neuronal communication will particularly benefit from miniaturization of control logic and real-time patient specific protocols.

- **Remote supervision,** for patients, handicapped and elderly people, using multi-parameters biosensors and tele-monitoring networks will improve the quality of the clinical environment and personal home. Through the same technologies, new mass markets are to be addressed for the clinical care and wellness of the patient. A key economic goal is the reduced cost of hospitalisation and the monitoring of elderly people requiring prolonged medical care using point-of-care terminals. To aid these transitions, new packaging technologies will be needed to use polymers and not glass for cartridges and platforms. Additionally, new IT networks in e-health hospitals will cut healthcare costs by enabling patients to get diagnosis and treatments anywhere at any time.
- **Fastest access** with the right treatment in emergency situations will save minutes of searching for rescue teams and reduce risks in emergency cases. Localisation techniques and electronically available personalized health data support efficient and targeted care actions. Localisation techniques support as well the freedom of to be supervised persons and the management in large hospitals in knowing where the nearest experts and expensive equipment is located.
- Finally, the huge potential for parallelisation and performance of the nanoelectronics will directly benefit the **analytical and research laboratories** in providing tools order of magnitude more efficient. This status will enable rapid progress in healthcare techniques thanks to a more efficient screening of the drug potential of new chemical compound therapeutic potential using bio-electronic devices, creating synergy between high volume laboratory-based systems for advanced treatments, and more cost effective home based systems.

Synergy with other priorities

From this sub-programme on “Healthcare and the Aging Society” there are possible synergies with:

- SP1 on Automotive as car safety can be improved by enabling wellness applications in an automotive environment (such as a sensor network that can monitor the driver’s vital signs and act accordingly). Also, imaging systems can benefit from new power electronic devices developed for electrical and hybrid vehicles.
- SP2 on Wireless Communication as the available of cheap and reliable wireless communication links can be essential in the realization of home patient monitoring and for improvements in advanced imaging systems for screening. Additionally, there can be synergy on the technology for LTE terminals to support safety on the road and safety at home.
- SP3 on Energy Efficiency as low-power techniques can be essential for monitoring systems that use portable or on-body devices, and new materials, devices and equipment for solar energy conversion can be beneficial to develop new radiation conversion detectors.
- SP4 on Design Methods & Tools as low levels of acceptable energy consumption and high levels of reliability are required for the complex heterogeneous systems for Healthcare applications.
- SP5 to create the best solution as a More than Moore spearhead for low-cost cartridges and platforms for microfluidics and gas sensors to monitor the body and environment.

Expected impact

Economic impact

The European medical / healthcare expenses amount for 12% of the GDP and the citizens who are 65+ years old, may contribute to 60% of the global healthcare budget. The proposed target activities support the reduction of the increasing healthcare expenses in using modern nano-electronics to maintain the expenses at a level which can be supported by the society.
The biotech sector itself is very dynamic in Europe where the number of companies – esp. SME's – is growing fastest in the world. "e-Health" is estimated to account for 5% of the total EU Member States' health budget by 2010. The size of the world electronic market addressing this field was amounting 78 billions € in 2007 and is expected to grow by 32% by 2012. All these facts show the emergence of a new market of integrated semiconductor microcircuits, microsystems for microfluidics and new semiconductor devices, which all are expected to grow significantly in the coming years.
Next to collective healthcare spending through insurance companies, the aging population will play a considerable role as consumers of life supporting systems based on electronic devices.

Social benefit

The quest for better health and wellness of our European society calls for more sophisticated tools and methods in order to reach the high expected standard of living of an ageing population. There are many societal benefits to develop and use application specific nanoelectronics for healthcare and wellness. It ranges from efficient, easy to use and cheaper diagnostic techniques made available to the doctor and to the citizen in order to promote preventive actions – e.g. through environmental and food control and through early disease detection –, to patient- and therapy-specific tools made available to clinicians in real time in order to enhance the efficiency of the healthcare. Remote patient supervision using biosensors, bio-data analysis and communication technologies associated with home self care and patient management – e.g. the clinical environment – are other major opportunities for cost saving and better patient follow-up in an ageing society and for people requiring prolonged medical care.

Targeted approach

It is expected that projects addressing "Healthcare and the Aging Society" will be formed by consortia combining the expertise of large firms, SMEs and academic research centres.
These projects can either show a horizontal integration with the final user (e.g. clinical) or a vertical integration with equipment, materials and design providers so to build a solid technology base for Europe and establish standards.

Possible topics of projects:

In many respect this domain is emerging and opening significant opportunities, esp. for SME's. Besides few well-established markets, new applications and emerging solutions have the potential to evolve in mass markets. Rapid changes are expected in this field and as flexibility is needed in the definition of priorities and milestones, several projects are expected, devoted to the following target activities:

- Early diagnostic and prevention through integrated micro-nano sensors (such as biosensors and MEMS-based heterogeneous sensors) and imaging systems (both stationary and mobile)
- Medical imaging systems and biosensors for fast screening, smart diagnosis, personalized therapy and low-invasive interventions
- Systems for remote patient treatment, supervision and monitoring of patients, handicapped and elderly people
- Personal assistance for people with limited mobility, sight or hearing abilities
- Tools for healthcare analysis and smart drug delivery, based on nanotechnology
- Biosensors for environmental monitoring

2.8 Summary

The JU Research Strategy defined in 1.2 is based on the fact that the draft MASP identifies the most important challenges to address from the economic, societal and political viewpoint and selects the most promising ones in terms of market success and lasting impact. The selected topics should ensure a broad participation of the Member States, while the projects should encompass the complete value chain, from technology development to applications that would yield commercially successful products.
The topics and proposals could be grouped synergetically in four major areas:

1. Advances in electric mobility
This topic encompasses the development of controllers, sensors, and specialized components for car safety, process technologies, packaging and SiP technologies satisfying specific automotive requirements, design methodologies including specific features such as predictive reliability, energy efficiency etc.
The subjects are included in SP1, SP3, SP4, SP5 and SP6.
2. Applications driving advances in n and n+1 CMOS technology nodes and their derivatives, related packaging and design technologies
Wireless communications (agile tranceivers, cognitive radio, 3D Integration, novel non-volatile memories etc.), energy efficiency in design and in control applications, health care and bio sensing, energy-aware design methodologies for complex components and systems etc.
The subjects are included in SP2, SP3, SP4, SP5, SP6 and SP7.

3. Energy efficient, ecologically benign future manufacturing technologies
This topic addresses specifically the equipment industry working on advances in specific modules such as substrates, lithography, metrology, inspection, efficient manufacturing, 450mm, etc.
The subjects are included in SP5 and SP6.

4. Alternative energies value chain and efficient power grid
Progress in energy conversion devices, circuit and system design, metering and appliances, lighting etc.
The subjects are included in SP3, SP4 and SP5.

3 Requirements for the submission of proposals

A proposal should satisfy the following requirements:

i. Each proposal should address at least one Sub-Programme

ii. All projects to be supported will be expected to identify, at proposal stage, their intended contribution to the achievement of the ENIAC SRA and AWP targets. Proposals should describe how projects would measure their contribution and how they would establish a baseline and thereafter monitor their progress compared with the baseline.

iii. All projects are expected to have a strong industrial focus and present a realistic context for industrially relevant, short to medium term research and technology development, and to enable its validation. All projects should demonstrate their expected industrial, social or economic impact.

iv. Clear expression of the technical approach to the research objectives will be essential.

v. All projects to be supported will be expected to share requirements and emerging results, during project execution, so as to achieve the coherent, synergistic progress sought by the ENIAC JU. All projects should demonstrate their possible synergy with other priorities, target initiatives or Sub-Programmes.

vi. Project consortia must be balanced. Considering the explicit involvement of SMEs and favoring clustering of SMEs in innovation eco-systems is encouraged.

vii. In view of the downstream research focus of the ENIAC JU and the targets described in this document, projects with duration longer than 3 years must provide adequate justification for their duration, relative to the application demonstrators and expected impact they describe.

4 Implementation of Call in 2010

4.1 Call 3 - 2010

- Call title: ENIAC Call 2010
- Identifier: ENIAC-2010-1
- Indicative date of publication:.26.02.2010
- Evaluation procedure:
  - Deadline for submission of Project Outlines: 30.04.2010
  - Deadline for submission of Full Project Proposals: 30.07.2010
- The submission of an eligible Project Outline is mandatory for the submission of a Full Project Proposal.
- The general eligibility criteria as well as evaluation criteria and sub-criteria are set out in chapter 5 of this work programme.
- Indicative timetable:
  - The ENIAC Joint Undertaking will provide the applicants with an assessment of Project Outlines by 28.5.2010
  - It is expected that the selection of Full Project Proposals for funding will take place in September 2010
  - It is expected that the negotiations for the selected proposals will start in late September 2010
- Project agreements: Participants in any project resulting from this call are required to conclude a project agreement.
- Financial contribution of the ENIAC Joint Undertaking to participants in projects: Following the evaluation, selection and award procedures of the ENIAC Joint Undertaking, the ENIAC Joint Undertaking will conclude grant agreements with participants. The financial contribution of the ENIAC Joint Undertaking will be 16.7% of eligible costs incurred by participants to implement the projects.

4.2 ENIAC Call 2010 budget

	Indicative Budget of Call 2010 (M€)
ENIAC Joint Undertaking [5]	30,14
ENIAC member States	54,80
Total indicative budget of Call	**84,95**

[5] estimated as 55% of the amount committed by ENIAC member States to the budget of this Call.

5 Eligibility and Evaluation Criteria for Proposals

5.1 Eligibility checks

The following eligibility criteria will be checked by the ENIAC Joint Undertaking:

1. Eligibility Criteria for proposals (Project Outlines and Full Project Proposals)
2. Eligibility Criteria for funding of individual participants (ENIAC JU funding and national funding from ENIAC Member States)

5.2 Eligibility Criteria for Proposals

Project Outlines (PO)

A PO will only be considered eligible if it meets all of the following conditions:

- It is submitted using the proposal service specified by ENIAC in the Guide for Participants
- It is received by the ENIAC JU before the deadline given in the call text for POs.
- It involves at least 3 non-affiliated legal entities established in at least 3 ENIAC member States[6]
- It is complete (i.e. both the requested administrative forms and the proposal description are present).
- It is submitted in English[7].
- The content of the PO relates to the topic(s) described in this work programme.

Full Project Proposals (FPP)

An FPP will only be considered eligible if it meets all of the following conditions:

- The corresponding PO has been considered eligible by the ENIAC JU
- It is submitted using the proposal service specified by ENIAC in the Guide for Participants
- It is received by the ENIAC JU before the deadline given in the call text for FPPs.
- It involves at least 3 non-affiliated legal entities established in at least 3 ENIAC member States.
- It is complete (i.e. both the requested administrative forms and the proposal description are present).
- It is submitted in English[8].
- The content of the FPP relates to the topic(s) described in this work programme.

[6] Currently: (Austria, Belgium, Czech Republic, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, the Netherlands, Norway, Poland, Portugal, Romania, Slovak Republic, Spain, Sweden and the United Kingdom)

[7] Except for the additional information and forms that may be requested by ENIAC member States for the verification of eligibility of national funding that can be in their respective national languages

[8] Except for the additional information and forms that may be requested by ENIAC member States for the verification of eligibility of national funding that can be in their respective national languages

5.3 Eligibility Criteria for funding

1. The ENIAC JU will carry out the verification of participants against the pre-defined Joint Undertaking eligibility criteria for funding as set out in the financial regulation or published in the Call, on the basis of verifications carried out by the Commission. These verifications will be performed as much as possible before applicants submit a Full Project Proposal.

2. The ENIAC JU will carry out the verification of participants from ENIAC member States and their contribution to the project proposals, on the basis of verifications carried out by the respective national authorities, against the pre-defined national eligibility criteria for funding as published in the Call. The verifications by national authorities will be done as much as possible before applicants submit a Full Project Proposal.

The full details on the eligibility criteria for funding will be published in the Call.

5.4 Evaluation criteria

Project Outline

The Project Outline will be assessed by the ENIAC JU, on the basis of the following criteria:

- Relevance will be considered in relation to the topic(s) of the work programme open in a given call and to the objectives of a call.
- Relevance and contribution to the overall ENIAC targets listed in section 3.
- Soundness of the concept
- Clarity and quality of the objectives and expected results
- Contribution, at the European and/or international level, to the expected impacts listed in the work programme under the relevant sub-programme
- Degree of application innovation in the context of the sub-programmes addressed
- Expected market impact of the results for the industrial partners
- Quality of the consortium as a whole including complementarities, balance and involvement of SMEs

Full Project Proposal

The evaluation criteria against which proposals will be judged are set out in the document ENIAC-PAB-4-08: "ENIAC Joint Undertaking selection and evaluation procedures related to Calls for proposals".

The 5 evaluation criteria are:

1. Relevance and contributions to the objectives of the Call.
2. R&D innovation and technical excellence.
3. S&T approach and work plan.
4. Market innovation and market impact.
5. Quality of consortium and management.

Evaluation scores will be awarded for each of the five criteria, and not for the sub-criteria. Each criterion will be scored out of 10. Criteria 1, 2, 3, and 5 will have a weight of 1 and criterion 4 will have a weight of 2. The threshold for the individual criteria (1), (2), (3), (4) will be 6. There

is no threshold for the individual criterion (5). The overall threshold, applying to the weighted sum of the five individual scores, will be 40.

Some further explanation on the evaluation criteria:

1. Relevance and contributions to the objectives of the Call.
    - Relevance will be considered in relation to the topic(s) of the work programme open in a given call and to the objectives of a call.
    - Relevance and contribution to the overall ENIAC targets listed in section 3.

2. R&D innovation and technical excellence.
    - Soundness of the concept
    - Clarity and quality of the objectives and expected results
    - Progress beyond the state-of-the-art.

3. S&T approach and work plan
    - Quality and effectiveness of the S&T methodology
    - Quality of the work plan.

4. Market innovation and market impact
    - Contribution, at the European and/or international level, to the expected impacts listed in the work programme under the relevant sub-programme
    - Market impact and quality of the exploitation plans of the industrial partners; quality of the market analysis section including competitor descriptions and market opportunities.
    - Appropriateness of measures for the dissemination of project results.
    - Contribution to standards.
    - Management of intellectual property.

5. Quality of consortium and management[9].
    - Appropriateness of the management structure and procedures
    - Quality and relevant experience of the individual participants
    - Quality of the consortium as a whole including complementarities, balance and involvement of SMEs
    - Appropriateness of the level, allocation and justification of the resources to be committed (budget, staff, equipment)

[9] This evaluation criterion corresponds to the **selection criteria** in the meaning of the general financial regulation (article 115) [OJ L 248, 16.09.2002, p. 1] and its implementing rules (article 176 and 177) [OJ L 357, 31.12.2002, p.1] and of the financial rules of the Joint Undertaking (article 101). It will also be the basis for assessing the 'operational capacity' of participants. The other four evaluation criteria (1-4) correspond to the **award criteria.**

6 How to submit a proposal

Proposals should be submitted in accordance with the terms set out in the call for proposals. In order to submit a proposal, applicants should consult the following documents:

- The text of the call for proposals, as announced in the Official Journal of the European Union and published on the webpage of the ENIAC Joint Undertaking
- This Work Programme
- ENIAC Eligibility criteria
- The Guide for Applicants

7 References

There are also a number of other useful texts which applicants could refer to:

AENEAS Articles of Association (http://www.eniac.eu)
Council Regulation 72/2008 (http://eur-lex.europa.eu)
ENIAC Multi-Annual Strategic Plan
Strategic Research Agenda of the European Technology Platform ENIAC (http://www.eniac.eu/web/downloads/SRA2007.pdf);
White book of Eureka cluster CATRENE: (http://www.catrene.org/web/calls/whitebook2.php)