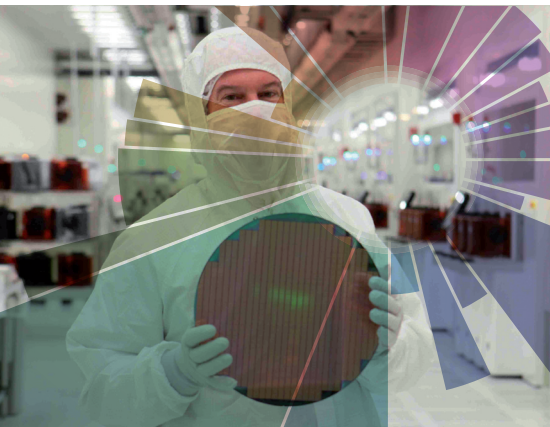


Project profile

INTEGRATE

Integrated Solutions for Agile Manufacturing in High-mix Semiconductor Fabs



Maintaining and developing a profitable and consistent manufacturing base in Europe is of key strategic relevance both in economic and political terms. The ENIAC JU project INTEGRATE shall enhance the wafer fab efficiency by improving the overall cycle time, decreasing the equipment cost of ownership, enabling simultaneous management of standard and non-standard lots and enhancing product quality. This will be achieved thanks to state of the art advances in manufacturing sciences and to reinforced collaboration within the local/regional ecosystems.

Sub Programme

- Equipment, Materials and Manufacturing



Objectives

European IC manufacturers are on the way to become suppliers of customized products for OEM companies, which means high flexibility and product diversity. INTEGRATE aims to enable IC production lines to efficiently manage a high product and technology mix and heterogeneous lots of different size and priority for development, engineering and prototyping. To reach these objectives research will be conducted to support the development of new manufacturing procedures, new organizations and new information and control tools. INTEGRATE will develop integrated process control and equipment control optimization tools, together with advanced lot flow control techniques that interact with lower and upper decisions levels but also consider various elements of the fab (tool status, auxiliary resources, qualifications etc.).

Work and consortium

INTEGRATE will focus especially on:

- data acquisition and analysis concepts
 - factory information and control system
 - and process data analysis from heterogeneous sample
- in order to develop procedures that can be implemented on existing fab information and control system, improving the management of heterogeneous work-in-progress and increasing the quality and processing speed of fast lots, while maximizing the total fab throughput.
- Actually, the project builds upon the algorithms developed in the previous project IMPROVE to make the move from “reactive” to “predictive” operations (ITRS Roadmap) to go further by addressing the needed improvements for the high mix production environment. The progress will be achieved by putting the pieces together and lifting them to the fab level, by adapting the day-to-day manufacturing rules and habits to the new operation methodologies. This will help bridging the gap between novel control

- factory operation methodologies

technologies and the operators and engineers running the fabs.

The research activities will be preceded and supported by survey workshops to summarize the status and detailed requirements at the user sites and to transform those specifications into general architectures. This will support the sustainability of the R&D activities and help to avoid island solutions and duplication of development efforts. The consortium includes major IDMs operating wafer fabs in Europe, equipment manufacturers, and a strong network of institutional and academic researchers.

Expected results

Measurable results are expected in various areas of the factory efficiency:

- Improvement of the fab capacity and overall cycle time (estimated with a constant equipment set) by providing the means for a better usage of the production equipment and optimizing the lots trajectory
- Decrease of the cost of ownership of the equipment thanks to a better management of the maintenance, qualifications and spare parts
- Improved simultaneous management of standard and non-standard lots by focusing on the problems of high-mix manufacturing and process data analysis from heterogeneous sample
- Increased product quality, especially for hot lots, thanks to advanced process control and data and yield analysis developments - better usage of the production equipment and optimizing the lots trajectory

Impact

The strategic nature of the semiconductor industry has been recognized around the world, and this recognition has led to the continuous emergence of new geographic regions as future semiconductor hubs, strongly supported by local governments. In fact, a competitive manufacturing semiconductor industry can act as a powerful engine for economic growth and high quality jobs. In addition, it provides an adequate incentive to reinforce the presence of upstream industries such as semiconductor equipment manufacturers and materials providers. The association of R&D activities with volume production and strong manufacturing facilities has a profound impact in developing local ecosystems.

The capability for Europe to maintain and develop a profitable and consistent manufacturing base is of key strategic relevance both in economic and political terms. INTEGRATE will help overcoming this challenge by

- Contributing to the competitiveness of the semiconductor fabrication in Europe thanks to an excellence level in manufacturing science
- Reinforcing local/regional ecosystems with an efficient collaboration scheme.

This will finally have a positive impact on direct and indirect employment and the reinforcement of the regional clusters and pan-European manufacturing network.

Equipment, Materials and Manufacturing

Partners

- STMicroelectronics (Crolles 2) SAS
- Micron Semiconductor Italia Srl
- Micron Technology Italia srl
- STMicroelectronics (Rousset) SAS
- STMicroelectronics Srl
- INTEL PERFORMANCE LEARNING SOLUTIONS LIMITED
- NXP Semiconductors Netherlands BV
- GLOBALFOUNDRIES Dresden Module One LLC & Co. KG
- Ecole Nationale Supérieure des Mines de Saint-Etienne - Centre Microélectronique de Provence
- Institut Polytechnique de Grenoble - Laboratoire GSCOP
- Université Claude Bernard Lyon 1
- Université d'Aix-Marseille - Laboratoire LSIS
- Probayes SAS
- Université Joseph Fourier Grenoble 1 - Laboratoire TIMC-IMAG
- Adixen vacuum products
- CamLine Datensysteme GmbH
- National University of Ireland Maynooth
- Politecnico di Milano
- Techno Fittings Srl
- Università Cattolica del Sacro Cuore
- Università degli studi di Milano Bicocca
- Università degli studi di Pavia
- XENIAProgetti Srl
- CNR-IMM
- NEDERLANDSE ORGANISATIE VOOR TOEGEPAST NATUURWETENSCHAPPELIJK ONDERZOEK - TNO
- Avisi B.V.
- Technische Universiteit Delft
- ASM International N.V.

Project co-ordinator:

- François Finck, STMicroelectronics

Key project dates

- Start: 01.01.2013
- Finish: 31.12.2015

Countries involved:

- France
- Germany
- Ireland
- Italy
- The Netherlands

Total budget:

- € 27,6 million



The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.

Details correct at time of print but subject to possible change. Updates will be included in the project summary at the end of the project.

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