CALL 2009

Project profile

ESiP

Efficient silicon multi-chip system-in-package integration – reliability, failure analysis and test

The ENIAC JU project ESiP is addressing the issues of reliability, failure analysis and testing in innovative system-in-package (SiP) solutions. Highly integrated systems with greater miniaturisation and increased functionality open new markets and improve the quality of life through a wide range of applications. In particular, higher systems integration technologies using multi-chip packaging, through-silicon via technologies or package-stacking approaches are growing in importance. Market studies show that SiP devices will have an average growth of 10 to 20% per year over the next five years.

Sub Programme

- Equipment and Materials for Nanoelectronics

Over the past decade, mass production of micro-/nanoelectronics devices has been moving out of Europe. While automotive and communications domains are still European strongholds, many mass-produced devices, such as memory, have been taken over by non-European producers. One option for bringing volume semiconductor production back to Europe is to establish highly-automated fabrication plants. This would require considerable capital investment and government subsidies, while having only a relatively small positive impact on employment.

A complementary strategy is to increase innovation, especially for nanoelectronics development in the field of homogeneous and – even more – heterogeneous 3D integration. Europe is in a leading position at the global start of a technology that will offer similar opportunities to those of classic CMOS scaling. It is strategically critical for Europe to develop sound intellectual property in this emerging field to maintain existing employment, develop replacement products and reap financial benefits and wealth.

Essential hardware enabler

Nanoelectronics will be the essential hardware enabler for future electronic products. These products will require ever greater systems integration with enhanced functionality and further miniaturisation. This increasing integration can be achieved using various technologies. The ENIAC JU project ESiP is focusing on silicon-based systems-integration technologies combined with appropriate system-in-package (SiP) solutions.

ESiP will work on reliability and failures as well as investigating the testing of high-density silicon multi-chip integration. The project starts at the silicon level but includes interaction between the chip/package system and the printed-circuit board, which will become more and more important in the future.

Partners from within the full value chain will participate. They include

major European chipmakers, systems houses, test- and analytical-equipment suppliers, and material suppliers, all committed to the achievement of project targets.

Innovative class of SiPs

ESiP focuses on equipment, materials and processes with the aim of developing an entirely new class of SiPs. There are four main objectives:

1. Reliability with respect to new methods and technologies including the whole chain from chip to package to board/system. This provides outstanding new opportunities for integration of digital, analogue, sensing or micro- and nano-electromechanical system (MEMS/NEMS) functions;
2. Failure analysis and metrology involving detailed investigation and development of inspection and analysis tools. Studies will be made of new failure mechanisms, innovative failure analysis equipment and methods for analysis of 3D integration of SiPs with MEMS;
3. Final testing of single and multi-chip packages involving new test approaches and equipment to ensure the functionality of SiPs in a cost-effective way, such as testing for KGD, will be integrated with design-for-test methodologies; and
4. SiP test vehicles will be assessed in terms of system reliability and potential risks as well as solutions to secure long-term stability. These test devices will also be used to evaluate innovative failure analysis methods/equipment and new test methods/equipment.

Strong strategic relevance

This ENIAC JU project has a strong strategic relevance for Europe. It follows the challenging trend to 'More than Moore' in micro-/nanoelectronics to develop a wide range of complex system-on-chip and SiP solutions. These incorporate not just digital circuitry but analogue, mixed signal and radio-frequency blocks as well as sensors and MEMS.

The ESiP approach will ultimately allow the partners to combine their specific technologies with MEMS/NEMS and novel high-performance devices as the most important steps towards heterogeneous integration. Such integration has been identified as one of the most important technology domains in the ENIAC JU Strategic Research Agenda.

The knowledge and expertise contributed by the consortium partners are complementary and form the basis for development throughout the complete value chain. Joining forces on a European transnational level is an integral feature of this project and an important step towards the development of More than Moore devices.

Strengthening leadership

Combining the forces of leading players in the European semiconductor industry is a major achievement in itself. The enthusiasm with which these competing companies have agreed to share their expertise and experience in this ENIAC JU project is a demonstration of their desire to contribute jointly to the strengthening of European leadership in the SiP market on a global scale.

Equipment and Materials for Nanoelectronics

Partners:

- 3D PLUS
- Advanced Laser Separation International
- AIT Austrian Institute of Technology
- austriamicrosystems
- Austrian Centre for Electron Microscopy and Nanoanalysis
- Boschman Technologies
- Cascade Microtech Dresden
- CEA-LETI
- CEA-LITEN
- Conpart
- Delft University of Technology
- EADS France
- EV Group E. Thallner
- Feinmetall
- Fraunhofer IWM
- Fraunhofer IZM
- IMEC
- Infineon Technologies
- InfraTec Infrared Measurement Division
- Melexis
- NXP Semiconductors Netherlands
- Okmetic
- Philips Lighting
- Picosun
- Point 35 Microstructures
- PVA TePla Analytical Systems
- Quantemol
- SensoNor Technologies
- Siemens
- Sintef
- SPEA
- STMicroelectronics France
- STMicroelectronics Italy
- Team Nanotec
- Technoprobe
- TNO
- Tronico-Alcen
- University College London
- University of Bologna, Alma Mater Studiorum
- VTI Technologies
- VTT Technical Research Centre of Finland

Project co-ordinator:

- Klaus Pressel, Infineon Technologies

Key project dates:

- Start: May 2010
- Finish: April 2013

Countries involved:

- Austria
- Belgium
- Germany
- Finland
- France
- Italy
- The Netherlands
- Norway
- United Kingdom

Total budget:

- €36.5 million

The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.

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