CALL 2010

Project profile

ARTEMOS

Agile radio-frequency transceivers and front-ends for future smart multi-standard communications applications

To provide mobile users with multiple services, today's cell phones simply include additional radio frequency (RF) circuitry for each band. Signal variability and the limitations of current technologies and conventional architectures make an integrated solution impossible. An RF front-end which covers all bands and meets all specifications requires homogeneous or heterogeneous integration of a set of tuneable architectures enabled by innovative technologies. The ENIAC JU project ARTEMOS aims to develop new techniques in simulation and modelling to create a new generation of multi-standard cell phones.

Sub Programme

- Nanoelectronics for wireless communications
- Nanoelectronics for energy efficiency
- Silicon process and integration for nanoelectronics

Mobile communications are evolving towards personal networks providing ubiquitous availability of services to transfer anything at anytime, anywhere, to anyone, via any path available, using a pocket-sized device. Consequently, there is a market pull by an increasingly connected world population asking for mobile access to vast information resources through the Internet via mobile phones, competing with a market push from an industry delivering all kinds of communications standards, products and applications

Currently, integrated multi-standard solutions for mobile phones are impossible because of severe signal integrity constraints and the limitations of current technologies and systems architectures. Consequently, the radio-frequency (RF) front-end includes additional circuitry for each band. If this trend continues, such an approach will eventually lead to an unsustainable size/cost increase due to the growing number of standards and frequency bands that would need support.

Agile RF capacities

The ENIAC JU project ARTEMOS has therefore brought together leading European mobile phone and integrated circuit (IC) specialists to develop agile RF transceiver capacities in future mobile radio communications products. The primary objective of these new architectures and technologies will be to manage multi-standard – multi-band, multi-data-rate and multi-waveform – operations with high modularity, low-power consumption, high reliability, high integration levels, low costs, reduced printed circuit board area and a reduced bill of materials.

This will not simply require smart RF architectures in CMOS and bi-polar CMOS (BiCMOS) technology but also the incorporation of microelectromechanical systems (MEMS) technologies. Achieving the integration of such complex structures requires advances in the design technology,

in particular novel simulation methodologies.

Key objectives include:

- Definition, implementation and verification of frequency agile – more than ten bands – multi-mode, multi-standard RF architectures, functions and system-on-chip solutions suitable for nanoscale (Bi) CMOS technologies; and
- Specification, development and characterisation of RF MEMS, tuneable filters, aerials and matching circuits within such RF architecture, meeting low cost, wide-band, high dynamic range, digital friendliness and power-efficiency requirements.

Ensuring universal access

A successful outcome will enable the production of multi-standard, multi-band devices in the range from 0.3 to 5 GHz that integrate in a single radio architecture all current 2G, 3G and 4G mobile phone modes – GSM/EDGE, UMTS and LTE – plus additional wireless communications systems such as WiFi, GPS, WirelessHD, Wireless USB, near field communication, professional mobile radio and digital TV standards. It will involve the lowest number of external surface acoustic wave or bulk acoustic wave filters and power amplifiers.

These novel devices will be brought to the market at low cost by using a reduced number of external, tuneable components and a maximum level of silicon integration. An additional goal is to achieve the lowest possible power consumption by ultra-low power solutions for future generation ICs based on optimised low voltage micro-architectures.

Key innovations will include frequency-agile, digital-friendly RF architectures featuring high dynamic range, suitable for integration in nanoscale (Bi)CMOS together with tuneable filters. The complexity of this challenge will also involve advances in simulation techniques and modelling to address fully the variety of new technologies that are under consideration.

Next level of integration

To satisfy the demanding requirements of ubiquitous communications systems offering multiple standards cost-effectively, significant progress in state-of-the-art technologies will be essential. Innovations are required from technology to electronic design automation, device and circuit architecture to platform and system level.

In recent years, R&D efforts have greatly improved the maturity of RF-MEMS technologies. With their current performance capability, RF MEMS are now ready to be integrated into mobile handsets, where they will appear as the technology enabling the agile and reconfigurable front-end modules. The remaining integration limits will be addressed from the technology and systems angle.

With partners that are active in the full value chain, from semiconductor suppliers, system houses, application domain, research and universities, the ARTEMOS consortium is confident that the realisation of its ambitious objectives will help Europe to achieve technological leadership in several domains that are targeted by ENIAC JU.

Wireless communications

Partners:

- AALTO University
- ART
- Brno University of Technology
- Cavendish Kinetics
- Commissariat à l'Energie Atomique et aux Energies Alternatives
- Danube Mobile Communications Engineering
- DelfMEMS
- Ecole Superieure d'Electricité
- Fachhochschule Hagenberg
- Fachhochschule Kärnten
- Foundation for Research and Technology Hellas
- IMC Austria
- Institut Telecom France
- Instituto de Telecomunicações
- Integrated Systems Development
- Iquadrat Informatica
- Johannes Kepler Universität Linz
- Lantiq A
- LEAT-CNRS
- Numonyx Italy
- NXP Semiconductors Belgium
- NXP Semiconductors France
- NXP Semiconductors Netherlands
- PULSE Finland
- ST-Ericsson (Grenoble)
- ST-Ericsson AT
- ST-Ericsson Belgium
- ST-Ericsson Netherlands
- ST-Ericsson R&D
- Technische Universiteit Delft
- Technische Universiteit Eindhoven
- TESLA, akciova spolecnost
- THALES Communications
- THALES Italia
- Universitá Degli Studi di Perugia
- Universitat Politecnica De Catalunya
- Uppsala Universitet
- Valtion Teknillinen Tutkimuskeskus

Project co-ordinator:

- Thomas Simonis, Danube Mobile Communications Engineering

Key project dates:

- Start: April 2011
- Finish: March 2014

Countries involved:

- Austria
- Belgium
- Czech Republic
- Germany
- Greece
- Finland
- France
- Italy
- The Netherlands
- Portugal
- Spain
- Sweden

Total budget:

- €40.9 million

Details correct at time of print but subject to possible change. Updates will be included in the project summary at the end of the project.

ENIAC Joint Undertaking • Brussels • Belgium
Tel : +32 2 221 81 02 • email: eniac@eniac.europa.eu • website: www.eniac.eu