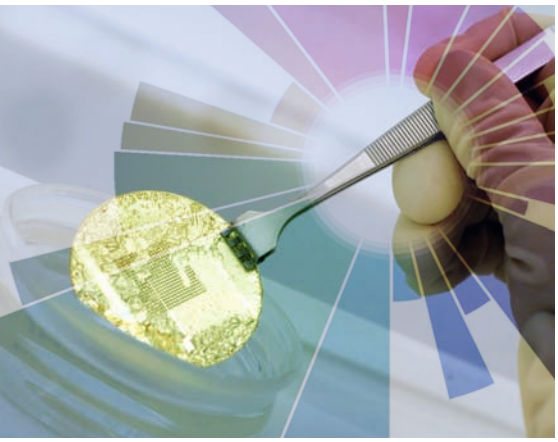
CALL 2010

Project profile

# PARSIMO

## *Partitioning and modelling of system-in-package*



Sensors, powerful processors, power drivers and radio-frequency (RF) interfaces are required as component parts in many application domains such as aerospace, automotive, automation, healthcare and consumer electronics. As the demand for smaller, smarter and cheaper modules grows, system-in-package design is seen as an enabler of new applications, especially incorporating mixed-signal systems, sensors and RF devices. The ENIAC JU project PARSIMO has brought together leading European specialists to speed design, automate production and develop a whole new range of advanced heterogeneous devices.

### Sub Programme

- Design methods and tools for nanoelectronics
- Silicon process and integration for nanoelectronics
- Nanoelectronics for automotive and transport
- Nanoelectronics for wireless communications
- Nanoelectronics for energy efficiency

Integration in heterogeneous system-in-package (SiP) designs results in smaller, smarter and more energy-efficient products. By making use of SiP designs, even small and medium-sized enterprises (SMEs) can gain access to the development of technologically advanced, miniaturised products. However, to date, the lack of appropriate design methodologies and flows has hindered the efficient development of SiPs.

The main goal of the ENIAC JU project PARSIMO is to organise tools and methodologies to improve design efficiency for complex devices needed in critical applications. Such devices often require the integration of heterogeneous logic components such as microprocessor cores, digital signal processors, memories and dedicated logic as well as heterogeneous functions – RF, analogue and power circuits – on-chip or in-package.

### *Models and methods*

PARSIMO will develop models and modelling methods to improve the predictive accuracy for sensitive SiP parts while reducing simulation time. In addition, the project will investigate partitioning methods to optimise cost, performance and power at early design stages.

Successful and efficient SiP design requires that the entire functionality is considered from simulation of the electrical behaviour to the structure of individual elements. While the former needs to be optimised, the latter is still very immature.

For the SiP approach, complex electronic functionality has to be partitioned into blocks to provide sub-functionality with clearly defined interfaces for data exchange. Dedicated software tools will be developed for partitioning. These will handle complex functionality and break it into sub-circuits based on existing components. Furthermore, those tools will define the interfacing procedures between the sub-circuits.

PARSIMO will investigate:

- Methods to facilitate partitioning in terms of system costs, perfor-

mance, etc.;
- Modelling methods that can handle the high complexity of SiP;
- Interfaces for MEMS and sensors;
- SiP design rules and language for a defined interface between designers and manufacturers; and
- Electronic design automation and computer-aided design tools filling the current gap in SiP design.

## *Shortening time to market*

PARSIMO will significantly speed-up SiP design with reduced time-to-market and lower overall design costs. Furthermore, by cutting manufacturing costs, the SiP approach will enable highly-integrated systems to be produced economically in the small to medium volumes typical for applications in areas such as transport, automation and wireless sensor networks.

Automotive, avionics and wireless electronics are characterised by very demanding boundary conditions. The harsh electrical environment requires input and output circuitry that can sustain extremely high voltage peaks. Motor control units and power amplifier units have to handle up to 80 V. The increasing demand for additional functions in modern cars can only be met by greater integration density achieved with scaled-down devices. However, smaller devices are much more sensitive to voltage, so special protection techniques are necessary.

For electronic parts, customers demand extended functionality and robustness against over voltages. However, automotive electronics are subject to very high cost pressures so cost-efficient manufacturing strategies are mandatory. A single technology often cannot satisfy in a cost-effective way all these contradictory requirements. SiP allows for the implementation of different technologies, each one at its best cost-performance capability, in a compact system.

## *Supporting SiP ecosystem*

Standardisation is an important goal of PARSIMO to support an SiP ecosystem which will allow all actors to exchange design data smoothly, including SMEs, large integrated device manufacturers, research institutions and universities. PARSIMO will contribute to establish the SiP concept as a third track for realising highly complex electronic systems as an alternative to printed circuit boards and system-on-chip devices. The most important advantages will be short times to market and low production costs.

The short design phase made possible by the evolution of the design automation tools, coupled with cost-efficient manufacturing, will allow SMEs and large companies to develop and fabricate new multi-purpose applications. This approach to efficient system design and manufacturing will generate significant job opportunities in Europe.

## Design methods and tools for nanoelectronics

### Partners:
- Coventor
- ESIEE Engineering
- Institute of Electron Technology (ITE)
- ENSICAEN/LaMIPS
- SARAS Technology
- Silvaco Europe
- Thales Airborne Systems
- University of Sheffield
- Wroclaw University of Technology

### Project co-ordinator:
- Maria Merlyne De Souza, University of Sheffield

### Key project dates:
- Start: March 2011
- Finish: June 2014

### Countries involved:
- France
- Poland
- United Kingdom

### Total budget:
- €4.9 million

*Details correct at time of print but subject to possible change. Updates will be included in the project summary at the end of the project.*



ENIAC Joint Undertaking • Brussels • Belgium
Tel : +32 2 221 81 02 • email: eniac@eniac.europa.eu • website: www.eniac.eu